IN THE SPECIFICATION

Please replace the paragraph beginning on page 3, line 19 with the following:

The tag memory control unit stores ~~effectiveness~~ validity determination information used to determine whether a cache memory address, which indicates an address of the sub memory block corresponding to the cache memory block and the data stored therein, and the cache memory block are ~~effective~~ valid or not.

Please replace the paragraph beginning on page 5, line 12 with the following:

Step (d) further comprises (d1) determining whether data stored in the cache memory block is ~~effective~~ valid, (d2) reading data from the memory block corresponding to the read address and writing data to the cache memory block if data stored in the cache memory block is not ~~effective~~ valid, (d3) updating information on the data written to the cache memory block, (d4) if data stored in the cache memory block is ~~effective~~ valid, reading data from the memory block corresponding the read address and writing ~~effective~~ valid data stored in the cache memory block to the memory block, and (d5) writing data to the cache memory block and updating information on the data written to the cache memory block.

Please replace the paragraph beginning on page 9, line 4 with the following:

If the next write address WADD and the next read address RADD are identical to each other and the next write address WADD and the next read address RADD are identical to the previous write address WADD and the previous read address RADD, it is necessary to perform a data write operation in the cache memory block CMB2. In this case, it has to be determined whether data already written in the cache memory block CMB2 is ~~effective~~ valid or not.

Please replace the paragraph beginning on page 9, line 10 with the following:

If the data already written in the cache memory block CMB2 is ~~effective~~ valid, it is read out and written in a sub memory block corresponding to the memory block MB2, and data corresponding to the next write address WADD is written in the cache memory block CMB2. ~~Effectiveness~~ Validity determination information, which indicates the ~~effectiveness~~ validity of data stored in the cache memory block CMB2, is stored in the tag memory control unit 210.

Please replace the paragraph beginning on page 12, line 12 with the following:

If neither the write address nor the read address is identical to the cache memory address, in step 510 it is determined whether data stored in the cache memory block is ~~effective~~ valid.

Please replace the paragraph beginning on page 12, line 20 with the following:

If data stored in the cache memory block is not ~~effective~~ valid, in step 540, data is read from the memory block corresponding to the read address and written to the cache memory block.

Please replace the paragraph beginning on page 12, line 23 with the following:

If data has to be written to or read from the sub memory block, priority is given to a data read operation. Thus, data is read from the sub memory block of the memory block MB2 corresponding to the read address RADD. Since data stored in the cache memory block CMB2 is not ~~effective~~ valid, data is written to the cache memory block CMB2.

Please replace the paragraph beginning on page 13, line 9 with the following:

If data stored in the cache memory block CMB2 is ~~effective~~ valid, in step 520, data is read from the memory block corresponding to the read address, and the data stored in the cache memory block CMB2 is read and written to the corresponding memory block.

Please replace the paragraph beginning on page 13, line 17 with the following:

Since the data stored in the cache memory block CMB2 is ~~effective~~ valid, the data stored in the cache memory block CMB2 is read, and the read data is written in the sub memory block corresponding to the read data. Then, in step 530, data is written in the cache memory block CMB2 in response to the cache control signal CCLS, and information on the data written in the cache memory block CMB2 is updated. The update of the cache data information is performed by the tag memory control unit 310.

Please replace the paragraph beginning on page 14, line 26 with the following:

Therefore, data is read from the cache memory block CMB2 in response to the cache control signal CCLS and then written to the sub memory block corresponding to the write address in response to the decoding control signal DCLS. Since the data is supposed to be written to the cache memory block CMB2 but is written to the sub memory block, the data stored in the cache memory block CMB2 is not ~~effective~~ valid. Therefore, information on the data stored in the cache memory block CMB2 is updated by the tag memory control unit 310.

Please replace the paragraph beginning on page 16, line 3 with the following:

Therefore, data is read from the cache memory block CMB2 in response to the cache control signal CCLS and then written to the sub memory block corresponding to the write address in response to the decoding control signal DCLS. Since the data is supposed to be written to the cache memory block CMB2 but is written to the sub memory block, the data stored in the cache memory block CMB2 is not ~~effective~~ valid. Therefore, information on the data stored in the cache memory block CMB2 is updated by the tag memory control unit 310.

IN THE DRAWINGS

Figure 3 is being changed to show the connection for reading data out of CMB2 and into an SMB. A proposed drawing correction accompanies this response.